AMENDMENTS TO THE CLAIMS

1-58. (Canceled)

59. (New) A method of generating a latency drift signal comprising the steps of:

generating a first signal for indicating that data requested has been received;

generating a plurality of derivative signals from said first signal, said plurality of derivative signals corresponding to a plurality of states of said first signal at a respective plurality of times;

comparing at least two of said derivative signals; and

generating a latency drift signal when said at least two of said derivative signals exhibit a predetermined relationship.

60. (New) The method of claim 60 further comprising inputting said plurality of derivative signals into a plurality of delay circuits.

61. (New) The method of claim 60, wherein said at least two of said derivative signals are compared using an OR gate.

62. (New) The method of claim 60, wherein said latency drift signal is used to determine a latency drift in a memory circuit.

63. (New) The method of claim 60, wherein said derivative signals are delayed relative to said first signal.

64. (New) The method of claim 63, wherein each of said derivative signals is delayed relative to a preceding derivative signal.

65. (New) A method of generating a latency drift signal comprising the steps of:

receiving a master clock signal at a first clock input of a latency detection circuit, said master clock signal being adapted to indicate a first start time of a signal response window, said signal response window including a first time interval of a first duration;

receiving a transaction status signal at a second transaction status input of said latency detection circuit during said first time interval;

sampling a state of said transaction status signal with said latency detection circuit at a plurality of sampling times within said first time interval; and

receiving a latency status signal from said latency detection circuit at a control device, said latency status signal corresponding to a state of said transaction status signal at one or more of said plurality of sampling times.

66. (New) The method of claim 66 further comprising indicating to said control device a moderate latency increasing status by said received latency status signal.

67. (New) The method of claim 66 further comprising indicating to said control device an excessive latency increasing status by said received latency status signal.

68. (New) The method of claim 66 further comprising indicating to said control device a moderate latency decreasing status by said received latency status signal.

69. (New) The method of claim 66 further comprising indicating to said control device an excessive latency decreasing status by said received latency status signal.

70. (New) The method of claim 66, wherein said plurality of sampling times comprises at least four sampling times.

71. (New) A latency drift detector comprising:

means for receiving a ready signal of a programmable response time memory component whose response time is being measured;

means for generating a plurality of data outputs indicating a respective time within a response window from a plurality of clock signals;

means for determining a latency drift based on said plurality of data outputs; and

means for recalibrating at least one programmable response time memory component when said determined latency drift exceeds a predetermined threshold.

72. (New) The detector of claim 71, further comprising a messaging means for indicating to a user a status of said memory component.

73. (New) The detector of claim 71, wherein said determining means utilizes long term averaging.

74. (New) The detector of claim 71, wherein said determining means utilizes short term averaging.

75. (New) The detector of claim 71, wherein said determining means generates latency drift data for a plurality of memory components.

76. (New) The detector of claim 75, wherein said latency drift data is utilized for preventative maintenance.

77. (New) A method of increasing reliability of an electronic system comprising:

receiving a master clock signal at a first clock input of a latency detection circuit, said master clock signal being adapted to indicate a first start time of a signal response window, said signal response window including a first time interval of a first duration;

receiving a transaction status signal at a second transaction status input of said latency detection circuit during said first time interval;

sampling a state of said transaction status signal with said latency detection circuit at a plurality of sampling times within said first time interval;

receiving a latency status signal from said latency detection circuit at a control device, said latency status signal corresponding to a state of said transaction status signal at one or more of said plurality of sampling times; and

servicing a component corresponding to said transaction status signal based on a state of said latency status signal received at said control device.

78. (New) The method of claims 77, wherein said servicing a component comprises replacing said component.

79. (New) The method of claims 77, wherein said servicing a component comprises transferring said component from a preferred system environment to a non-preferred system environment.

80. (New) The method of claims 77, wherein said servicing a component comprises transferring said component from a non-preferred system environment to a preferred system environment.

81. (New) The method of claims 77, wherein said servicing a component comprises notifying a user of a status of said component.

82. (New) The method of claims 77, wherein said servicing a component comprises calculating a latency time statistic corresponding to said status of said component.

83. (New) The method of claims 82 further comprising storing a latency time interval value in a system memory.